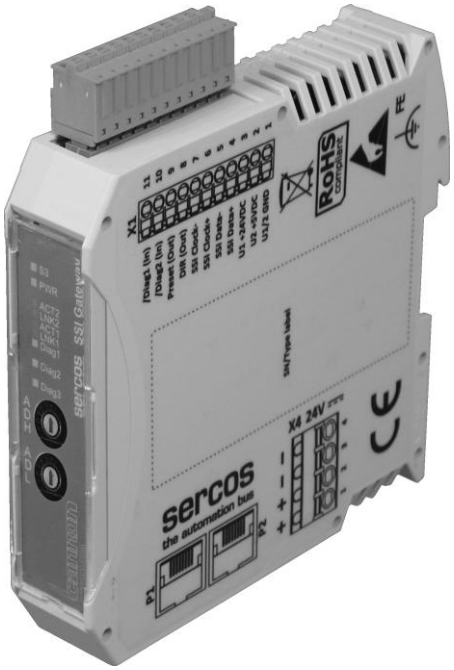
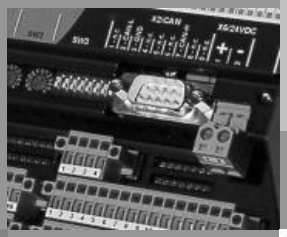
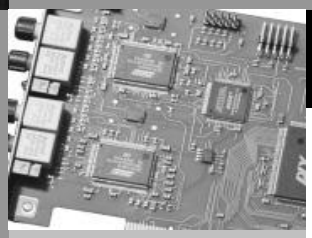






SSI-Gateway

Order code: 70069300

Manual

cannon AUTOMATA

Document information

Author	Thomas Straßer
Version	V1.3/07.03.13
File	E:\Projekte\Automata\S2SSI\Documents\E-70069300-G-A-V010.doc
Content	Order code: 70069300

Revision status

Date	Author	Description
16.07.2012	T. Strasser	Creation
09.11.2012	Ch. Melzer	Product picture replaced
14.1.2013	Ch. Melzer	Mistake in IDN "Encoder control" corrected
24.2.2013	Ch. Melzer	Error codes added, some minor corrections

CANNON-Automata

Automata GmbH & Co. KG
Gewerbering 5
D-86510 Ried
Phone +49 (0)8233-7916-0
FAX +49 (0)8233-7916-99
info@automata.de

Automata S.p.A.
Via G. Carducci, 705
I-21042 Caronno Pertusella (VA)
Phone +39 (02)9639970
FAX +39 (02)96399731
welcome@automata.it

www.cannon-automata.com

Content

Figures

Tables

1 Scope

This document describes the SSI-Gateway (order code: 70069300). The device is used as interface between encoders with SSI protocol (Synchron Serial Interface) and sercos III real-time Ethernet networks.

2 Functional description

The following picture shows the integration of a standard encoder with SSI protocol into a sercos III real-time Ethernet topology. The SSI-Gateway can be integrated with line or ring topologies.

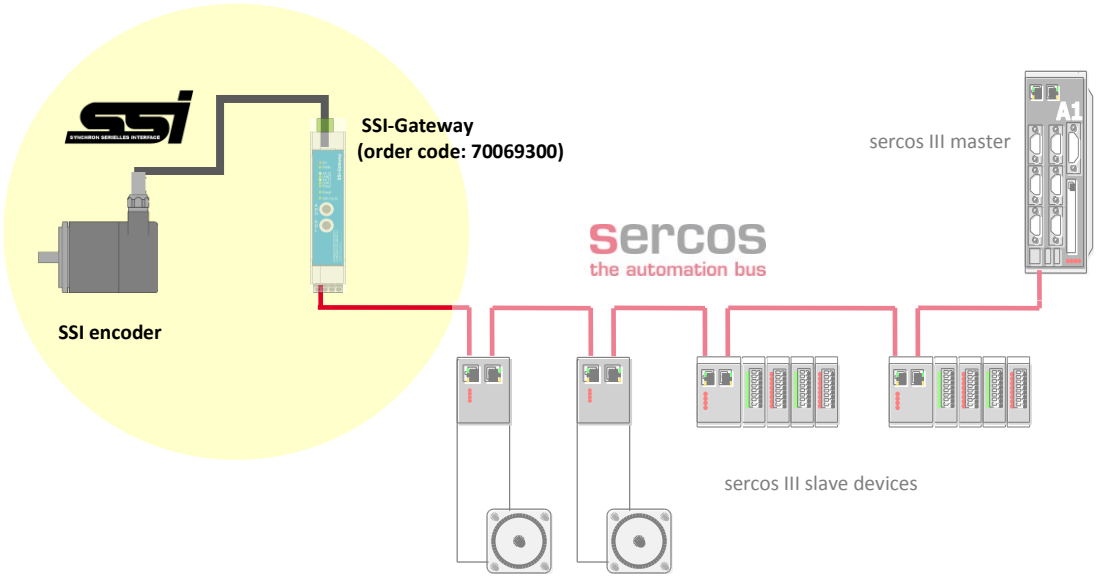


Figure 1: SSI-Gateway and SSI-Encoder connected to the sercos real-time Ethernet network

Features

- 1 x SSI port with 11p screw clamp terminal
- extensive SSI protocol settings
- sercos III slave interface with 2 x RJ45 connectors
- sercos III FSP-Encoder profile
- 9 diagnosis LEDs
- 2 rotary switches for sercos slave address
- 2 digital diagnosis inputs
- 2 digital outputs (e.g. preset encoder, switch over direction between CW and CCW)
- 24 VDC power supply
- 5 VDC and 24 VDC output for encoder supply

3 Product data

Order information	
Order code	70069300
Name	SSI-Gateway
Technical data	
Housing dimension (WxHxD) and material	22,5 x 114,5 x 99 mm; plastic
Mounting	DIN-rail mounting
Weight	120 g
Power supply	24VDC (19 – 30 VDC),
SSI	interface for one encoder with SSI protocol
sercos III	sercos III slave interface with FSP-Encoder

Table 1: Product data

3.1 Housing

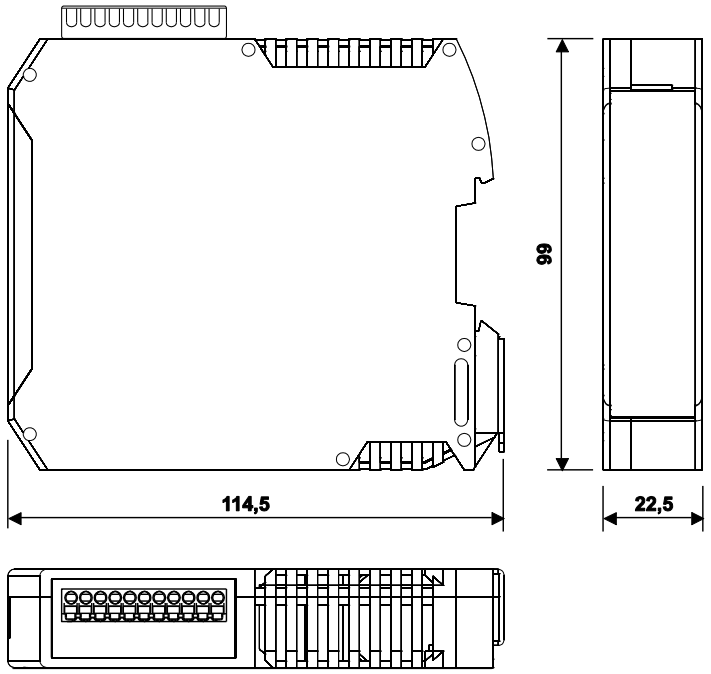


Figure 2: Housing dimensions (mm)

3.2 LEDs and controls

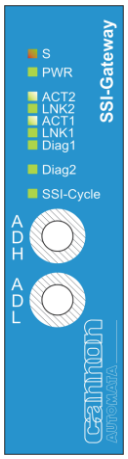
Name	Function	Picture
S	sercos III LED (see **3.4.7**)	
PWR	Power supply is ok (green)	
ACT2	Activity on sercos connector **P2** (green blinking)	
LNK2	Link on sercos connector **P2** (green)	
ACT1	Activity on sercos connector **P1** (green blinking)	
LNK1	Link on sercos connector **P1** (green)	
Diag1	Status of signal **/Diag1 (X4.11)** (green = signal is active, input is LOW)	
Diag2	Status of signal **/Diag2 (X4.10)** (green = signal is active, input is LOW)	
SSI-Cycle	SSI activity (green)	
ADH	Bit 8..15 of sercos device address (IDN/S-0-1040)	
ADL	Bit 0..7 of sercos device address (IDN/S-0-1040)	

Table 2: LEDs and controls (front side)

3.3 SSI hardware interface

The following table shows the SSI features:

Feature	Description	Connector.Pin (Signal name)
Signal type (Data and Clock)	RS422 galvanic isolated	X1.4 .. X1.7 (SSI Clock+/-, SSI Data +/-)
Supported transmission frequencies	67,5 kHz .. 2 MHz	-
Supported encoder resolutions	8 .. 31 bits	-
Code	Binary or Gray Code	-
Parity	none/odd/even	-
DataValid bit	on/off	-

Table 3: SSI features

3.3.1 Additional features of encoder interface

The following table shows the additional signals available on the encoder interface:

Feature	Description	Connector.Pin (Signal name)
Encoder power supply 24VDC	15 VDC/120 mA (short circuit protected)	X1.1 and X1.3 (U1/2 GND, U1 +24VDC)
Encoder power supply 5VDC	5 VDC/330 mA (short circuit protected)	X1.1 and X1.2 (U1/2 GND, U1 +5VDC)
DIR	Output signal with configurable signal level (0 .. 5 VDC or 0 .. 24 VDC). This signal is controlled over parameters of the sercos slave interface. Default use case is switching over the encoder counting direction (CW or CCW).	X1.8 (DIR)
Preset	Output signal with configurable signal level (0 .. 5 VDC or 0 .. 24 VDC). This signal is controlled over parameters of the sercos slave interface. Default use case is presetting the encoder (current position = 0).	X1.9 (Preset)
Diag2	This input signal can be used for diagnostic purposes. The sercos III master can read over a parameter.	X1.10 (/Diag2)
Diag1	This input signal can be used for diagnostic purposes. The sercos III master can read over a parameter.	X1.11 (/Diag1)

Table 4: Additional features of the encoder interface

3.4 sercos III interface

3.4.1 Basic features

Profile	Class, function group
SCP	SCP_VarCFG, SCP_Diag, SCP_Sync, SCP_NRT 4 connections (1 x MS, 1 x SM, 2 x CC)
GDP	GDP_Basic, GDP_PWD, GDP_Id, GDP_Rev, GDP_BKP
FSP-Encoder	Version 1.3-1.0 FG Encoder-Basic (1 encoder instance) (Features not supported: velocity measurement, acceleration measurement, vibration measurement, encoder temperature, 64bit position values, marker positions)
min. cycle time	250 µs
FPGA-/Firmware update	Compliant to sercos specification for firmware update over TFTP

Table 5: sercos III slave interface features

3.4.2 sercos III device address (IDN/S-0-1040)

The sercos III device address (IDN/S-0-1040) is defined over two rotary switches (ADH and ADL) on the front of the SSI-Gateway (see 3.2). The setting is only applied at transition from NRT mode to CP0. Changing the switches in other communication phases or writing the IDN/S-0-1040 over SVC has no effect on the device address. Nevertheless, the current switch position is always sown in IDN/S-0-1040. The default address is **1**.

ADL: Bit 0 .. 7 of the device address **(Default = 1)**

ADH: Bit 8 .. 15 of the device address **(Default = 0)**

3.4.3 UCC settings and capabilities

IDN	Name	Description
S-0-1019	MAC Address	*(unique for the device, not changeable)*
S-0-1020	IP Address	Default = **192.168.2.100** Changes over SVC are stored and become effective when entering the NRT mode.
S-0-1021	Subnet Mask	Default = **255.255.255.0** Changes over SVC are stored and become effective when entering the NRT mode.
S-0-1022	Gateway address	Default = **0.0.0.0** Changes over SVC are stored and become effective when entering the NRT mode.
S-0-1027.0.1	Requested MTU	Default = **1500** Changes over SVC are stored and become effective when entering the NRT mode.

Table 6: UCC settings

UCC (Unified Communication Channel) is only active while the communication phases NRT, CP0 and CP1. The following S/IP services and features are supported:

- Service "Reset (97)" (UDP/IP mode)
- Update over TFTP (see 3.4.8)

3.4.4 FSP-Encoder-Basic

The SSI-Gateway includes the FSP-Encoder-Basic with one encoder instance (= 1).

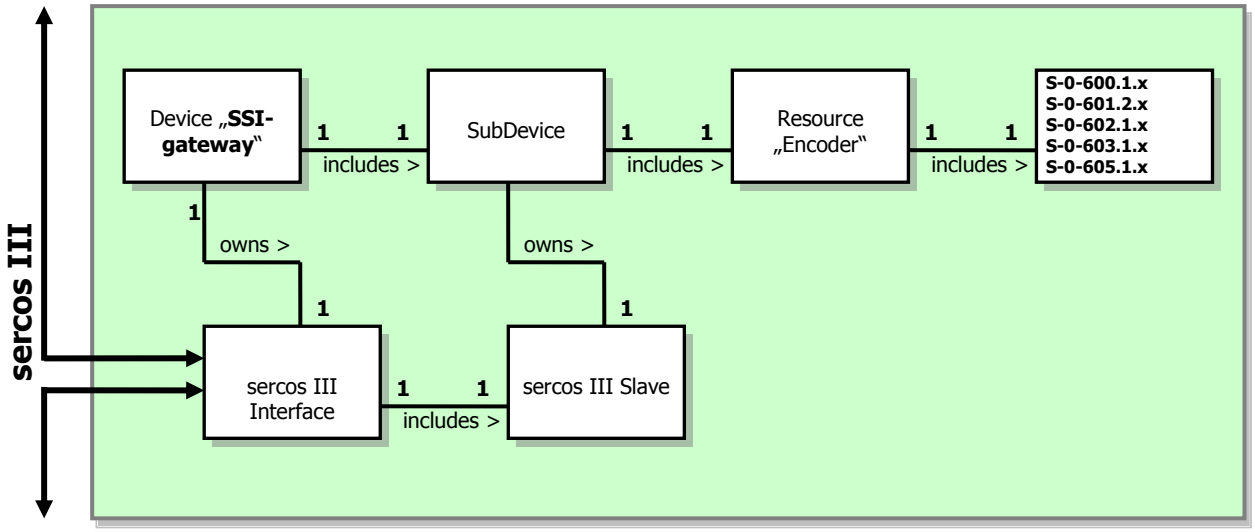


Figure 3: sercos III device model

Extensions to the FSP-Encoder-Basis

IDN	Name	Description
S-0-0601.1.128	Encoder selector	**Type:** parameter, 16bit, unsigned, decimal **Default:** 0 **Range:** 1 .. 7 **Function:** Encoder configuration data set that shall be activated over the procedure command IDN/S-0-0601.1.129.
S-0-0601.1.129	Activate encoder	**Type:** procedure command **Function:** With this procedure command, the master can activate one of the 7 encoder configuration data sets. The configuration data set to be activated is selected over the IDN/S-0-0601.1.128 (Encoder selector). The configuration data set IDN/S-0-0602.**x**.y is copied to IDN/S-0-0602.**0**.y. The SSI interface is initialized with this configuration data.
S-x-0602.1.128	Encoder vendor	**Type:** parameter, text **Default:** "(undefined vendor)" **Function:** Name of encoder vendor, e.g. "Baumer". **x** is in the range of [0 .. 7]
S-x-0602.1.129	Encoder order code	**Type:** parameter, text **Default:** "(undefined order code)" **Function:** Order code of the encoder, e.g. "GM400.AA2A002". **x** is in the range of [0 .. 7]
S-0-0603.1.128	SSI-Gateway diagnostic inputs	**Type:** parameter, 16bit, binary **Default:** - **Function:** Bit 0: status of signal "/Diag1" (X1.11) Bit 1: status of signal "/Diag2" (X1.10) *Bit 2 .. 7: (reserved)* Bit 8 .. 15: SSI cycle counter

Table 7: Extensions to the FSP-Encoder-Basic

Encoder configuration data sets

The SSI-Gateway has **8** configuration data sets: IDN/S-**0**-0602.1.y to IDN/S-**7**-0602.1.y. These data sets are stored in Flash-Memory. Data set 0 is active and must contain settings valid for the connected SSI encoder. Data sets 1 to 7 are not active and can contain settings for any other SSI encoder type.

The active data set 0 is used to initialize the SSI-Gateway hardware in the following states:

- Immediately after **power on**
- With procedure command **IDN/S-0-0127** (CP3 transition check)
- With procedure command **IDN/S-0-0601.1.129** (Activate encoder)
- With a write access to **IDN/S-0-602.1.x** (only while CP2)

The encoder configuration data sets are stored in Flash-Memory with the procedure command **IDN/S-0-0264** (Backup working memory procedure command)

IDN	Name	Description
S-x-0602.1.1	Phys. Encoder type	Bit 0 = 0: Rotational encoder **(default)** Bit 0 = 1: Linear encoder *Bit 1..15: (reserved)*
S-x-0602.1.2	Phys. Encoder properties	Bit 0 = 0: Graycode Bit 0 = 1: Binary code **(default)** *Bit 1..2: (reserved)* Bit 3 = 0: Data valid bit OFF **(default)** Bit 3 = 1: Data valid bit ON Bit 4..5 = b'00: No parity **(default)** Bit 4..5 = b'01: ODD parity Bit 4..5 = b'10: EVEN parity Bit 4..5 = b'11: *(reserved)* *Bit 6..7: (reserved)* Bit 8..15: Encoder frequency 0 = 67,5 kHz 1 = 100 kHz 2 = 125 kHz 3 = 200 kHz 4 = 250 kHz 5 = 300 kHz 6 = 400 kHz 7 = 500 kHz 8 = 600 kHz 9 = 700 kHz 10 = 800 kHz 11 = 900 kHz 12 = 1 MHz **(default)** 13 = 2 MHz Bit 16..23: Encoder resolution 0 = 8 bit 1 = 9 bit 2 = 10 bit 3 = 11 bit 4 = 12 bit 5 = 13 bit 6 = 14 bit 7 = 15 bit 8 = 16 bit 9 = 17 bit 10 = 18 bit 11 = 19 bit 12 = 20 bit 13 = 21 bit 14 = 22 bit 15 = 23 bit 16 = 24 bit 17 = 25 bit 18 = 26 bit 19 = 27 bit 20 = 28 bit 21 = 29 bit **(default)**

			22 = 30 bit 23 = 31 bit >=24 = *(reserved)*
		Bit 24:	Voltage level of the signals "Preset" and "DIR" 0: 5VDC **(default)** 1: 24VDC
		Bit 25:	Polarity of the encoder signal "Preset" 0: HIGH active **(default)** 1: LOW active
		Bit 26:	Polarity of the encoder signal "DIR" 0: HIGH active **(default)** 1: LOW active
		Bit 27..31:	*(reserved)*
S-x-0602.1.3	Phys. Encoder resolution (incremental)	8192 **(default)**	
S-x-0602.1.4	Phys. Encoder resolution (absolute)	8192 **(default)**	
S-x-0602.1.7	Phys. Encoder protocol configuration	0 *(reserved)*	

Table 8: Encoder configuration

3.4.5 Product specific IDNs

IDN	Name	Description
S-0-1300.0.128	FPGA register BOARD-ID	Board ID
S-0-1300.0.129	FPGA register SYSID-ID	SYSID-ID of the FPGA content
S-0-1300.0.130	FPGA register SYSID-Timestamp	SYSID-Timestamp of the FPGA content
S-0-1300.0.131	Configuration data-set identification	Identification string of the configuration data set
S-0-1300.0.132	Firmware checksum	Checksum of the firmware
S-0-1300.0.133	Firmware filename	Filename of the firmware
S-0-1300.0.135	Slave communication stack	Identification string of the sercos III slave communication stack
S-0-1300.0.136	Application Build Info	Identification string of the firmware

Table 9: Product specific IDNs

3.4.6 Error and warning codes (IDN/S-0-0390)

Code	Text (IDN/S-0-0095)	Description
0x050E0100	"SSI wire break on data line(s)"	Wire break
0x050F0200	"SSI short circuit on data line(s)"	Short circuit on encoder signals
0x050E0300	"/Diag1 (X1.11) active" or "/Diag2 (X1.10) active"	One of the two diagnosis inputs has become active (LOW)

Table 10: Error and warning codes

3.4.7 sercos III LED

The following table shows the codes indicating the device status according to the sercos specification V1.3.

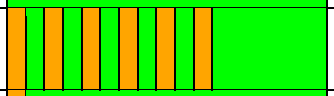
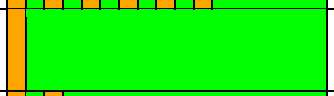
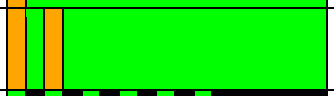
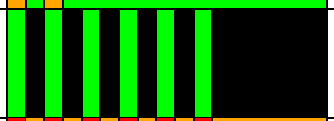
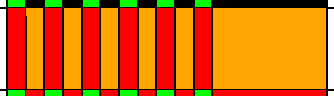
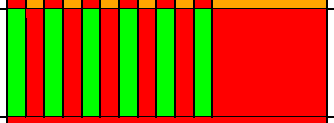
Pattern	Color	Description	Priority	Comment
#1	dark	NRT-Mode	0	no sercos communication
#2	orange	CP0	0	communication phase 0 is active
#3		CP1	0	communication phase 1 is active
#4		CP2	0	communication phase 2 is active
#5		CP3	0	communication phase 3 is active
#6	green	CP4	0	communication phase 4 is active
#7		HP0	1	device is in hot-plug phase 0
#8		HP1	1	device is in hot-plug phase 1
#9		HP2	1	device is in hot-plug phase 2
#10		Fast forward ⇒ Loopback	2	RT-state has changed from fast-forward to loopback
#11		application error	3	see GDP & FSP Status codes class error
#12		MST losses ≥ (S-0-1003/2)	4	as long as the communication warning (S-DEV.Bit15) in the Device status is present, at least 2 sec.
#13	red	communication error	5	see SCP Status codes class error
#14		Identification	6	Invoked by (C-DEV.Bit 15 in the Device Control) or SIP Identification request
#15		Watchdog error	7	application is not running
	-------- 3 sec -------			

Table 11: sercos III LED coding

3.4.8 Firmware update

For the update of device firmware the TFTP protocol is used. For this purpose the SSI-Gateway is equipped with a TFTP server.

Preconditions for error free functioning of the TFTP server:

- The device must be in NRT mode or in communication phase CP0 or CP1
- The device must have a valid MAC address (IDN/S-0-1019)
- The device must have a valid IP address (IDN/S-0-1020)
- The device must have a valid Subnet Mask (IDN/S-0-1021)

Restrictions of the TFTP server:

- A TFTP client cannot download files from the SSI-Gateway
- Files must be transmitted in binary mode (octet)
- The transmitted files must have the same name as defined in the IDN/S-0-1300.0.133 (Firmware filename), typically "ssi-gateway.bin".
- The following file extension are valid:
  - *.fpga FPGA content
  - *.bin device firmware
  - *.ini device configuration file

TFTP server error messages:

Error	Description
Access violation: Ongoing transmission in progress	While an ongoing file transmission an attempt was made to transmit another file. The TFTP server doesn't support simultaneous transmission of files.
Illegal TFTP operation: Read request not supported	An attempt was made to download a file from the SSI-Gateway.
Illegal TFTP operation: 0xYYYY	An illegal (undefined) TFTP op-code was received. The following op-codes are supported: • Read Request (1) • Write Request (2) • File Data (3) • Data Acknowledge (4) • Error (5)
Illegal TFTP operation: Awaiting <Filename X> but received <Filename Y>	A write request for file X was received. Now actually file data should follow, but instead a write request for file Y was received.
Unknown transfer ID: Wrong filename or extension: '<Received Filename>', '<Received Extension>' expected: '<Expected Filename …>'	A file with name <Received Filename> and extension <Received Extension> was received. However, the file <Expected Filename …> was expected.
Unknown transfer ID: Wrong Block#: <Block#X>, expected: <Block#Y>	While the TFTP transmission each block is enumerated. The number sequential and incremented by 1 with each block. This message indicates that a sequence error has occurred.
Unknown transfer mode: Allowed transfer mode: octet, used transfer mode: <Transfer Mode>	An attempt was made to transfer a file in a not supported mode. The TFTP server supports only binary mode (octet).
Disk full or allocation exceeded	It was not possible to allocate enough memory to save the received data.

Table 12: TFTP server error messages

Update process

The transmitted files are kept in RAM until the file containing the firmware (*.bin) is successful transmitted. Immediately after the successful reception of the firmware file all up to this moment transferred files (incl. firmware file) are programmed to flash memory.

If other files (*.fpga or *.ini) are successful transmitted a watchdog timer is started. If no other file transfer is started within 1 minute all up to this moment received data is discarded. This means that the firmware file always has to be transmitted as last.

After successful update the device remains in the current state. The device is not automatically re-launched.

Sample for a complete update (firmware, FPGA and configuration file) under Windows®:

```
c:\update_dir>tftp -i 192.168.2.100 PUT ssi-gateway.fpga
c:\update_dir>tftp -i 192.168.2.100 PUT ssi-gateway.ini
c:\update_dir>tftp -i 192.168.2.100 PUT ssi-gateway.bin
```

Sample for only updating the firmware under Windows®:

```
c:\update_dir>tftp -i 192.168.2.100 PUT ssi-gateway.bin
```

Visualization of the update process

State	Visualization
File transfer	LED **SSI-Cycle** is blinking: 0.3 sec ON, 0.1 sec OFF
Programming	LED **SSI-Cycle** is blinking: 0.1 sec ON, 0.4 sec OFF
Programming successful finished	LED **SSI-Cycle** permanent ON
Programming finished with error	LED **SSI-Cycle** is blinking: 0.2 sec ON, 0.2 sec OFF

Table 13: Visualization of the update process

Reset service

For a remote reset of the SSI-Gateway the S/IP service "Reset" (UDP/IP version) can be used (for details see S/IP specification).

4 Connectors and electrical characteristics

4.1 Connectors

4.1.1 SSI interface connector (X1)

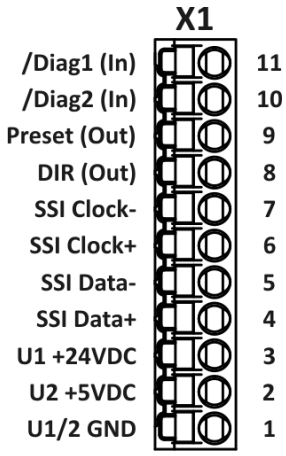
Pin	Signal	Picture
1	U1/2 GND	
2	U2 +5VDC	
3	U1 +24VDC	
4	SSI Data+	
5	SSI Data-	
6	SSI Clock+	
7	SSI Clock-	
8	DIR (Out)	
9	Preset (Out)	
10	/Diag2 (In)	
11	/Diag1 (In)	

Table 14: Pin allocation SSI interface connector (X1)

4.1.2 sercos III connectors (P1 and P2)

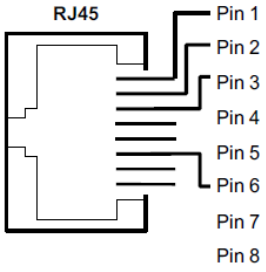
Pin	Signal	Picture
1	TxD+	
2	TxD-	
3	RxD+	
4	n.c.	
5	n.c.	
6	RxD-	
7	n.c.	
8	n.c.	

Table 15: Pin allocation sercos III ports (P1 and P2)

4.1.3 Power supply connector (X4)

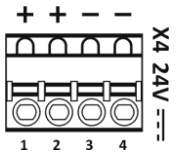
Pin	Signal	Picture
1	+24DVC	
2	+24VDC	
3	GND	
4	GND	

Table 16: Pin allocation power supply connector (X4)

4.2 Electrical characteristics

Power supply		
Nominal value	24 VDC	
Range	19 VDC .. 30 VDC (incl. ripple)	
Current consumption	max. 300 mA	
Encoder supply		
U1 +24VDC	max. load = 120 mA	
U2 +5VDC	max. load = 330 mA	
Output signals		
Preset, **DIR** **Preset** is eq. to **IDN/S-0-0605.1.1** (Encoder control) **bit 5** (set position raw value), whereas IDN/S-0-0601.1.8 is always 0. **DIR** is eq. to **IDN/S-0-0605.1.1** (Encoder control) **bit 3** (Direction polarity)	IDN/S-x-0602.1.2: Bit 24 = 0 (**Default**) **Signal level:** TTL **max. Load:** 0,5 mA	IDN/ S-x-0602.1.2: Bit 24 = 1 **Signal level:** 0 .. 24 VDC **max. Load:** 1,5 mA
Input signals		
/Diag1, **/Diag2** The sercos III master can get the status of the two signals over **the IDN/S-0-0603.1.128**, **bit 0 (/Diag1)** and **bit 1 (/Diag2)**	**Low level:** 0 .. 1,8 VDC **High level:** 2,7 .. 24 VDC max. input voltage is 24 VDC. Higher voltage can damage the device!	

Table 17: Electrical characteristic